



Docket No.: 4006-117

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

WU, BIING-SENG *et al.*

U.S. Patent Application No. 09/826,096

Filed: April 5, 2001

For: METHOD OF REDUCING FLICKERING AND INHOMOGENEOUS BRIGHTNESS IN LCD

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: Confirmation No. 2725
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: Group Art Unit: 2673
:
: Examiner: Nitin Patel

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

COMMISSIONER FOR PATENTS
P.O. Box 1450
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Sir:

The following are comments on the Examiner's statement of reasons for allowance found in the Notice of Allowance mailed November 16, 2006.

The Examiner in the statement of reasons for allowance seemed to inadvertently omit and/or incorrectly identify several aspects of the claimed invention, namely:

1. A scan line circuit that solves screen flicker, imperfect exposure junctions and inhomogeneous brightness in a TFT-LCD, which includes a plurality of perpendicular scan lines and a plurality of horizontal data lines, each of the scan lines connecting a plurality of pixel TFTs in a row and each of the data lines connecting a plurality of pixel TFTs in a column to form an array of the pixel TFTs, and a drain of the each pixel TFTs connecting a liquid crystal capacitor and a storage capacitor, wherein each of the scan line comprises: gate voltage deformation means for deforming a gate input voltage waveform input from an input terminal of the scan line, the gate voltage deformation means located only between the gate of the first pixel TFT in the row and the input terminal of the scan line, as recited in independent claim 13.

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2. A scan line circuit that solves screen flicker, imperfect exposure junctions and inhomogeneous brightness in a TFT-LCD, which includes a plurality of perpendicular scan lines and a plurality of horizontal data lines, each of the scan lines connecting a plurality of pixel TFTs in a row and each of the data lines connecting a plurality of pixel TFTs in a column to form an array of the pixel TFTs, and a drain of the each pixel TFTs connecting a liquid crystal capacitor and a storage capacitor, wherein each of the scan line comprises: gate voltage deformation means for generating a deformed gate voltage waveform transmitted to the pixel TFTs connected to the same scan line, the gate voltage deformation means located between the gate of the first pixel TFT in the row and the input terminal of the scan line, as recited in independent claim 18.

3. It should be further noted that independent claim 18 does not include "only" in its last paragraph, i.e., independent claim 18 should not be limited to include the feature of claim 13 that "the gate voltage deformation means located only between the gate of the first pixel TFT in the row and the input terminal of the scan line."

Respectfully submitted,

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